



inter chip key fuse encryption decryption register

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Results **1 - 2** of **2**. (0.11 sec)**Secure configuration of field programmable gate arrays**[psu.edt](#)

T Kean - Field-Programmable Logic and Applications, 2001 - Springer

... analysis prior art systems came to the conclusion that each FPGA **chip** should have ... The proposed security technology offers **key** advantages compared with alternative schemes: it does not ... A.Guccione, Delon Levi and Prasanna Sundararajan, "Jbits: A Java-based **Inter-** face for ...[Cited by 50](#) - [Related articles](#) - [BL Direct](#) - [All 17 versions](#)**Method of using a mask programmed **key** to securely configure a field ...**

TA Kean - US Patent App. 09/780,681, 2001 - Google Patents

... can be downloaded to the CSoC 50 through an industry standard Joint Test Action Group (JTAG)

inter- face and ... read out of on **chip** configuration memory 14 **encrypt** it and write it to the off-**chip**in-system ... This encryp- tion can use the ID value stored in the ID **register** as a **key**. ...[Related articles](#) - [All 4 versions](#)

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